Cross-couple DTMOS Rectifier with Floating sub-circuit using 65nm SOTB CMOS technology for uW RF Energy Harvesting

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Abstract This paper presents a design and evaluations of cross-couple rectifier with floating sub-circuit using DTMOS (Dynamic Threshold MOSFET) in uW input power. The circuit was fabricated in 65nm SOTB CMOS technology and evaluated in wide range of frequency, with various loads and small input power. The proposed circuit shows a better performance as compared to the conventional DTMOS rectifier. When input power is higher than -12 dBm, PCE of the proposed circuit becomes more than 20% and reaches maximum 33% at -5 dBm.

Keyword DTMOS, BTMOS, Cross-couple rectifier, RF Energy Harvesting.

1. INTRODUCTION

Energy harvesting system is an essential solution to eliminate battery for Internet of Thing (IoT) applications. RF rectifier which is used to convert RF input signal to DC output is a main part of the system [1]. Many researches try to increase power conversion efficiency (PCE) of CMOS rectifier circuit, but, in uW input power range, where input signal is smaller than threshold voltage (V_{th}) of MOSFET, PCE of circuit dramatically decrease. Some V_{th} cancellation techniques were proposed to boost PCE such as: static V_{th} cancellation technique [2], differential-drive topology [3], floating sub-circuit bias [4]. In [1] and [5], DTMOS is utilized and results show that the performance of circuit using DTMOS is better than rectifier using BTMOS.

In this paper, we propose Cross-couple DTMOS rectifier with floating sub-circuit. Circuit characteristics is compared with the same circuit configuration using BTMOS (Body tied to source MOSFET) and the other schemes using DTMOS rectifiers. The circuit was fabricated using 65nm SOTB CMOS because threshold of SOTB MOS can be changed larger than bulk, so that DTMOS become effective.

2. CIRCUIT DESCRIPTION

CMOS rectifiers using DTMOS are proposed in previous research [1], [5]. In [5], S. Shalesh implemented conventional DTMOS rectifier as shown in Fig1. In this scheme, DTMOS is defined as gate-drain-body tied together. Consequently, DTMOS is diode-connected MOSFET with controlled V_{th}.

Cross-couple CMOS rectifier scheme shows better performance than conventional CMOS rectifier [3], [4]. Cross-couple rectifier with floating sub-circuit scheme [4] is utilized to design in this paper. Fig 2 shows the proposed cross-couple DTMOS rectifier with floating sub-circuit. Configuration of DTMOS in proposed circuit is gate tied to body.

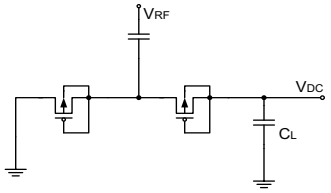

Fig.1. Conventional DTMOS rectifier [5]

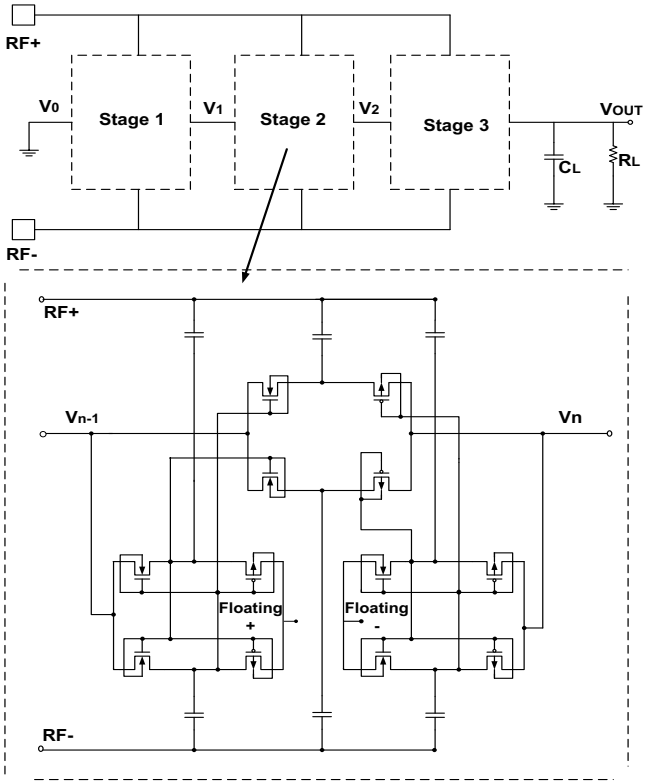

Fig.2. Cross-couple DTMOS rectifier with floating sub-circuit.

3. SIMULATION AND EVALUATION CONDITIONS

3.1. SIMULATION CONDITION

The circuit was designed using 65nm SOTB CMOS process. Proposed circuit consists of 3-stage cross-couple DTMOS rectifier with floating sub-circuit. W/L ratios of NMOS and PMOS in main-circuit are 2.4um/0.06um respectively

Fig 3 shows a simulation model of RF energy harvesting system. In this model, antenna is symbolized as voltage source in series with source resistor as antenna resistance ($R_S = 50\Omega$). Matching circuit is utilized to maximize input power to rectifier circuit.

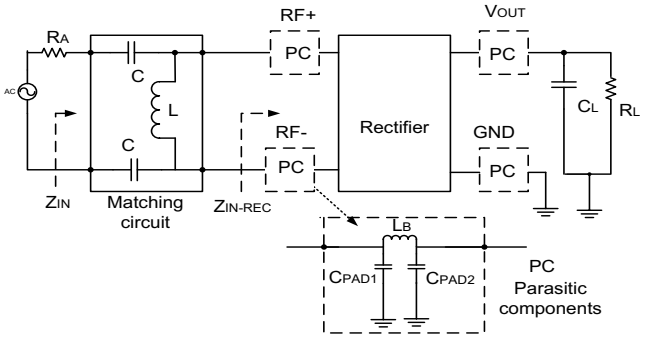

Fig.3. Simulation model of circuit

Simulation condition is considered with the effect of parasitic components of PCB board and chip. In each port of rectifier circuit has parasitic components as PC modeled in Fig 3. Bonding wire is equivalent to parasitic inductor L_B and is supposed to be 2nH. Pads are equivalent to parasitic capacitor C_{PAD1} and C_{PAD2} are supposed to be 1pF. Simulated input impedance Z_{IN_REC} at 800 MHz is $1-j*190$ then matching circuit is built as in Fig 3. Inductor L for matching is 33nH, and capacitor C_{PAD1} and C_{PAD2} are considered equal 64fF. No transmission line model is included in this simulation.

Power conversion efficiency (PCE) of circuit is

$$PCE(\%) = \frac{P_{OUT}}{P_{IN}}.100\% \quad (1)$$

calculated by equation (1)

Where P_{IN} is the power that antenna supply to the rectifier. Consider in ideal matching then $R_A = Z_{IN}$ so P_{IN} can be calculated by equation (2).

$$P_{IN} = \frac{P_A}{2} = \frac{V_A^2}{2R_A} \quad (2)$$

Where V_A is root mean square of input voltage.

P_{OUT} is output power of rectifier and can be calculated by equation (3)

$$P_{OUT} = \frac{V_{OUT}^2}{R_L} \quad (3)$$

3.2. EVALUATION CONDITION

Circuit was fabricated by using 65nm SOTB CMOS technology [6]. Fig 10 shows the PCB board.

Measurement set up is shown as in Fig 4. Input power is defined as RF input power from the signal generator to DUT. The core wire of cable is connected to RF+ port in DUT, copper shield of cable is connected to RF- point. Between RF+ and RF- we connect a capacitor to make a matching circuit. Output signal can be seen in oscilloscope RTO1024.

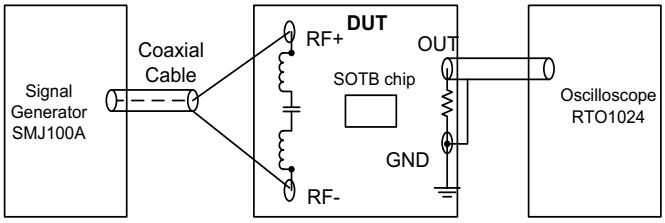

Fig.4. Measurement set up model

4. RESULTS

At 800MHz input frequency and 100kΩ load, output voltages of the proposed circuit and cross-couple DTNOS rectifier with floating sub-circuit [4] are shown as in Fig 5. Output voltage of circuit using DTMOS is higher than that of circuit using BTMOS.

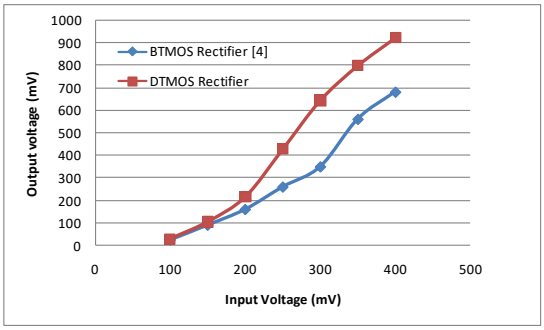

Fig.5. Simulated output voltages of DTMOS cross-couple rectifier and BTMOS cross-couple rectifier.

Fig 6 shows the measured PCE of the proposed circuit as a function of load. PCE of circuit is the highest when load is 10 kΩ and peak of PCE is 33% at -5 dBm input power.

Fig 7 shows the PCE comparison result between DTMOS conventional rectifier in [5] and the proposed circuit. Result shows that when input power is smaller than -10 dBm, PCE of the proposed circuit and DTMOS conventional rectifier are nearly the same. In a higher input power range (P ≥ -10 dBm), PCE of this work is much higher than that in [5], by 15 % higher at -5 dBm.

Fig 8 and Fig 9 show the comparison results between measurement result and simulation results of the proposed circuit in 10 kΩ load at 800 MHz input frequency. Output voltage and PCE of measurement

are higher than simulation. This may be because of the effect of parasitic components in PCB board to the whole circuit. Beside the effect of bonding wires and pads, transmission line also affects to circuit. This effect is needed to be investigated in future research.

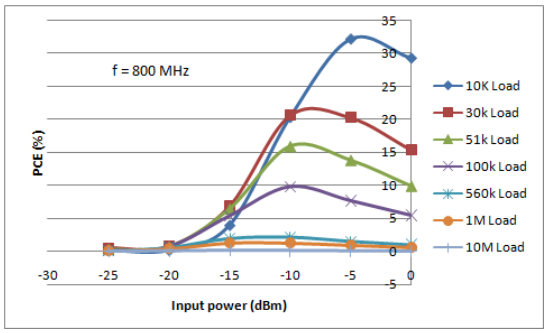

Fig.6. Measured PCE on various loads.

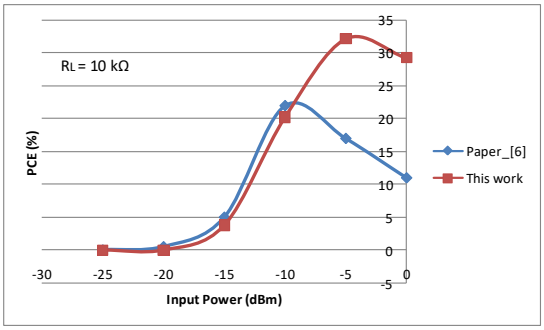

Fig.7. Measured PCE of the proposed circuit and conventional DTMOS rectifier [5].

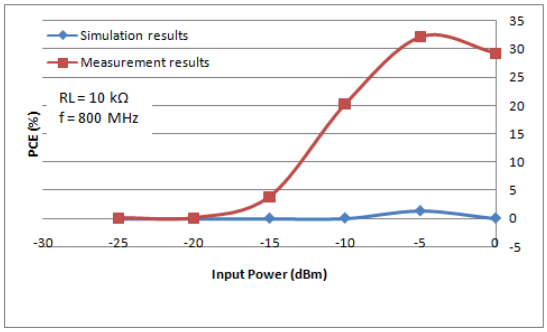

Fig.8. PCE results of simulation and measurement of the proposed circuit.

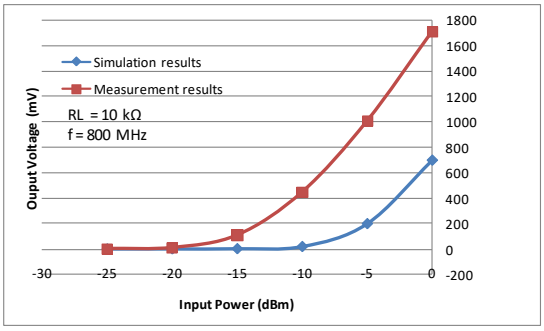

Fig.9. Output simulation and measurement output voltage of the proposed circuit

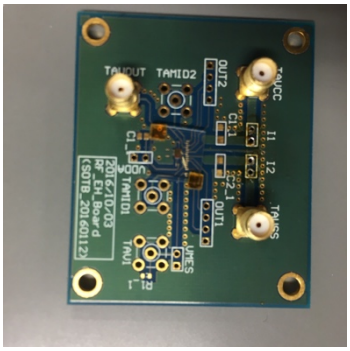

Fig.10. Cross-couple DTMOS rectifier chip.

5. CONCLUSION

Cross-couple DTMOS rectifier with floating sub-circuit is designed using 65nm SOTB CMOS technique and evaluated. A high PCE in small input voltage is achieved, 33 % PCE at -5 dBm input power. With the results shown in paper, DTMOS can apply in cross-couple CMOS rectifier to boost PCE of circuit. The proposed circuit is a good candidate for uW RF energy harvesting.

Acknowledgments

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